

5 **ON-CHIP INDUCTOR HAVING A SQUARE GEOMETRY AND HIGH Q FACTOR
 AND METHOD OF MANUFACTURE THEREOF**

10 **TECHNICAL FIELD OF THE INVENTION**

 This invention relates generally to integrated
circuits and more particularly to on-chip inductors and on-
chip transformers.

15 **BACKGROUND OF THE INVENTION**

 Integrated circuits (IC's) are known to include a
substrate, one or more dielectric layers on the substrate,
and one or more metal layers supported by a corresponding
20 dielectric layer. The metal layers are fabricated in such
a way to produce on-chip components such as resistors,
transistors, capacitors, inductors, et cetera. How an on-
chip component is fabricated and the physical limits placed
on on-chip components are dictated by the technology used
25 and foundry rules governing such technology.

 For example, CMOS technology is readily used for cost
effective integrated circuits. Foundries that manufacture
CMOS integrated circuits provide rules governing the number
30 of dielectric layers, number of metal layers, metal track
sizes, spacing between metal tracks, angular bends of metal
tracks, and other aspects of integrated circuit production.

 While CMOS technology and the corresponding foundry
35 rules allow on-chip inductors to be created, the quality

factor (i.e., the measure of a component's ability to produce a large output at a resident frequency and selectivity of the component) is limited to a value of 5-10. As is known, a circular trace pattern for an on-chip inductor theoretically has a greater Q factor than a square or rectangular trace pattern of similar inductance, but has a larger IC footprint and violates foundry rules. As such, circular on-chip inductors are not used.

To emulate the benefits of a circular on-chip inductor, while maintaining compliance with foundry rules, many integrated circuit designers use an octagonal inductor. However, an octagonal inductor is larger than a similar trace length square or rectangular inductor. As such, IC designers choose between larger octagonal inductors with a higher Q factor and smaller square or rectangular inductors with a lower Q factor. In some instances, an octagonal inductor is impractical due to its size and yet a square or rectangular on-chip inductor is impractical due to its low quality factor. And, in all instances, smaller on-chip inductors with similar performance characteristics are preferred over larger on-chip inductors.

Therefore, a need exists for a high quality factor rectangular and/or square on-chip inductor.

SUMMARY OF THE INVENTION

These needs and others are substantially met by the on-chip inductor and/or on-chip transformer disclosed herein. Such an on-chip inductor includes a dielectric

layer and a conductive winding on the dielectric layer. The conductive winding has a substantially square geometry and has at least its exterior corners geometrically shaped to reduce impedance of the conductive winding at a

5 particular operating frequency. Since the quality factor of an on-chip inductor is inversely proportional to the effective series impedance of the inductor at an operating frequency, by reducing the effective series impedance, the quality factor is increased. In addition, the inductor has
10 lower capacitance values in comparison to substantially equal inductors that do not practice the present invention, thus allowing the inductor of the present invention to have a higher self-resonance.

15 Other embodiments of the on-chip inductor include providing a geometric shaping of the internal and external corners at approximately 135° each. Alternatively, the interior angle of a corner may be approximately 90° while the exterior of the corner may be approximately 135° .

20 Further variations of the geometric shaping have multiple angles on the interior angle and multiple angles on the exterior angle. Still further embodiments of the on-chip inductor include having a spiral configuration for the conductive winding, having conductive windings on one or
25 more dielectric layers operably coupled together via metal bridges, and/or including a secondary winding to produce an on-chip transformer.

Such an on-chip conductor and/or on-chip transformer
30 may be manufactured by creating a dielectric layer and then creating a conductive winding on the dielectric layer. The conductive winding is created to have a substantially

square geometry where its corners are geometrically shaped to reduce impedance of the on-chip inductor at an operating frequency.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B illustrate an on-chip inductor in accordance with the present invention;

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Figures 2A and 2B illustrate an alternate embodiment of an on-chip inductor in accordance with the present invention;

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Figures 3A and 3B illustrate another embodiment of an on-chip inductor in accordance with the present invention;

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Figures 4A and 4B illustrate yet another embodiment of an on-chip inductor in accordance with the present invention;

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Figures 5A and 5B illustrate a further embodiment of an on-chip inductor in accordance with the present invention;

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Figures 6A and 6B illustrate yet a further embodiment of an on-chip inductor in accordance with the present invention;

Figures 7A, B and C illustrate an on-chip transformer in accordance with the present invention;

Figure 3 illustrates a logic diagram of a method for manufacturing an on-chip inductor in accordance with the present invention; and

5 Figure 9 illustrates a logic diagram of a method for manufacturing an on-chip transformer in accordance with the present invention.

DETAIL DESCRIPTION OF A PREFERRED EMBODIMENT

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Figures 1A and 1B illustrate an on-chip inductor 10 that includes a winding 12 on a dielectric layer 14. The winding 12 includes geometric shaping 16 at its exterior corners. As illustrated, winding 12 has a substantially square shape and may include one or more turns on one or more dielectric layers. By including the geometric shaping 16, the effective impedance at operating frequencies (e.g., 2.4 gigahertz) is reduced, thereby increasing the quality factor of on-chip inductor 10.

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In general, the inductance value of an on-chip inductor is dependent on the length of the interior edge of the metalization (i.e., the interior edge of winding 12) where the current tends to concentrate. Accordingly, the interior diameter of the inductor is the deciding factor for size minimization. As has been demonstrated in simulations, the highest current density is distributed on the interior edge of an inductor and gives the dominate contribution to the inductance. Note that the simulations were performed at 1.6 gigahertz and 2.4 gigahertz. As such, the inductance of an on-chip inductor is increased by increasing the length of its interior edge. This favors a

rectangular design rather than an octagonal one, occupying the same rectangular area on an integrated circuit and having the same track width.

5 To improve the quality factor of rectangular on-chip inductors and/or square on-chip inductors, current turbulence within the metal track needs to be reduced. Such turbulence consumes power as resistive loss, but does not contribute to the inductive value. Thus, by
10 eliminating, or reducing current turbulence, by cutting the corners of winding 12, the resistive loss due to turbulence is reduced and the inductance value is not affected. As such, by including the 135° corners on the exterior of the winding, as illustrated in Figures 1A and 1B, the current
15 turbulence is reduced, thus reducing resistive loss without effecting the inductance value. As is known, the quality factor for an inductor equals $2(\pi)fL/R$, where f is the operating frequency, L is the inductance, and R is the effective series resistance at the operating frequency.
20 Thus, by maintaining the same inductance value and reducing the effective impedance at the operating frequency, the quality factor is increased. In simulations, the quality factor has been improved by at least 5% and in general is improved by at least 20%. As such, on-chip inductor 10 has
25 the benefits over an octagonal inductor of similar inductance value in that it has a smaller integrated circuit footprint, can achieve similar inductance values and similar or greater quality factor values, and has lower capacitance values.

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Figures 2A and 2B illustrate an on-chip inductor 20 that includes winding 22 formed on dielectric layer 14.

Winding 22 includes geometric shape 26 at each of its corners. Winding 22 may be one or more turns on one or more dielectric layers to produce the on-chip inductor 20.

5 The geometric shape 26 has the interior and exterior angles of each corner being approximately 135° . As such, the geometric shaping 26 reduces the current turbulence within winding 22 and thus reduces the resistive loss without effecting the inductance value of on-chip inductor
10 20. As one of average skill in the art will appreciate, for the on-chip inductors of Figures 1 and 2, the geometric shaping 16 and 26 of 135° at the corners, is well within the current foundry rules for CMOS technology.

15 Figures 3A and 3B illustrate an on-chip inductor 30 that includes winding 32 created on dielectric layer 14. Winding 32 includes geometric shaping 36. In this embodiment, the geometric shaping 36 has angles on the interior and exterior corners of winding 32. The geometric
20 shaping, more closely approximates an octagon but does not create an octagonal shape. In comparison with on-chip inductor 20, on-chip inductor 30 has more deeply cut corners at 135° angles.

25 Figures 4A and 4B illustrate an on-chip inductor 40 that includes winding 42 created on dielectric layer 14. Winding 42 includes a spiral configuration that may be on one or more dielectric layers. As shown, each corner of winding 42 is geometrically shaped 36. In this example,
30 the geometric shaping is similar to the geometric shaping of Figure 1 where the external corners have 135° angles while the interior angles are 90° . As one of average skill

in the art will appreciate, the geometric shaping as illustrated in Figures 2A and 2B, and 3A and 3B may also be used with a spiral winding 42.

5 Figures 5A and 5B illustrate on-chip inductor 50 that includes winding 52 and dielectric layer 14. Winding 52 may be a single turn on a single dielectric layer, a spiral winding on a single dielectric layer, a single turn on multiple dielectric layers and/or multiple turns on
10 multiple dielectric layers.

As illustrated, winding 52 includes geometric shaping 56 on its exterior angles. In this illustration, the geometric shaping 56 includes multiple angles at the
15 corners. The angles for the geometric shaping 56 are dependent on allowable angle cuts per the foundry rules.

Figures 6A and 6B illustrate on-chip inductor 60 that includes winding 62 and dielectric layer 14. Winding 62
20 may be a single turn on dielectric layer 14, multiple turns on dielectric layer 14, multiple single turns on multiple dielectric layers or multiple turns on multiple dielectric layers.

25 As shown, each corner of winding 62 is geometrically shaped 66. In this illustration, the geometric shaping 66 includes multiple angles on both the interior corner and exterior corner of the corners of winding 62. Again, the angles for such multiple angles are dependent on allowable
30 foundry rules.

Figures 7A, B and C illustrate an on-chip transformer 70 that includes a primary winding 72 on dielectric layer 14, a secondary winding 74 on dielectric layer 78. The primary winding 72 at each of its corners includes
5 geometric shaping 76. The secondary winding 74 includes geometric shaping 76 at each of its corners. The geometric shaping 76 may include a single angular cut on each of its exterior corners (as shown in Figure 1), singular angle cuts on each of its interior and exterior angles (as
10 illustrated in Figures 2 or 3), multiple cuts on its exterior corners (as illustrated in Figure 5), or multiple angular cuts on its exterior and interior angles (as illustrated in Figure 6).

15 As one of average skill in the art will appreciate, each of the primary and secondary windings may be a single turn on a single layer, multiple turns on a single layer, multiple single turns on multiple layers, and/or multiple spiral turns on multiple layers.

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Figure 8 illustrates a logic diagram of a method for creating an on-chip inductor. The process begins at Step 80 where a dielectric layer is created on a substrate. The dielectric layer may be a silicon dielectric, gallium
25 arsenate, silicon germanium, and/or any other material used to fabricate integrated circuits.

The process then proceeds to Step 82 where a
conductive winding is created on the dielectric layer. The
30 creation of the conductive winding includes forming the winding to have a substantially square geometry and geometrically shaping its corners to reduce impedance of

the on-chip inductor at an operating frequency. The geometric shaping may be done as illustrated in Figures 1 through 3, 5, and 6. The fabrication of the conductive winding may be done as illustrated in Figures 1 through 6.

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Figure 9 illustrates a logic diagram of a method for creating an on-chip inductor. The process begins at Step 90 where a primary conductive winding that has a substantially square geometry is created on a 1st dielectric layer. The corners of the primary conductive winding are geometrically shaped to reduce impedance of the primary conductive winding at an operating frequency. The geometric shaping of the corners may be done as illustrated in Figures 1 through 3, 5, and 6.

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The process then proceeds to Step 92 where a secondary conductive winding that has a substantially square geometry is created on a 2nd dielectric layer. The corners of the secondary conductive winding are geometrically shaped to reduce impedance of the secondary conductive winding at an operating frequency. The geometric shaping of the corners may be done as illustrated in Figures 1 through 3, 5 and 6. As one of average skill in the art will appreciate, the creation of the primary and secondary windings may be done by forming a single turn on a single dielectric layer, forming a single turn on multiple dielectric layers, forming multiple turns on a single dielectric layer or by forming multiple turns on multiple dielectric layers.

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The preceding discussion has presented an on-chip inductor that has a substantially square geometry with an improved quality factor. As one of average skill in the

art will appreciate, other embodiments may be derived from the teachings of the present invention, without deviating from the scope of the claims.